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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,374	02/02/2000	Masami Kidono	OOCL-11 (11P024627)	6123

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EXAMINER

PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 07/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/496,374

Applicant(s)

KIDONO ET AL.

Examiner

Jeff Piziali

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 15 April 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.
2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on April 15, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.
3. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

## INFORMATION ON HOW TO EFFECT DRAWING CHANGES

### 4. **Correction of Informalities -- 37 CFR 1.85**

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings

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should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

**5. Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

**Timing of Corrections**

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-10 are rejected under 35 U.S.C. 102(a) as being anticipated by the current application's own admitted prior art.

Regarding claim 1, the background of the current invention discloses a solid-state imaging device comprising: a pixel unit [Fig. 7, 1] constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit [Fig. 7, 2] for vertically transferring charge from the pixels in the pixel unit; a horizontal transfer unit for horizontally transferring

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charge from the vertical transfer unit; shift gates [Fig. 7, 3] each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes [Fig. 7, 4A] for controlling the shift gates; and a plurality of lead lines [Fig. 7, 4B] and a plurality of connection terminals [Fig. 7, 6] for connecting the gate electrodes to an external circuit [Fig. 7, 5]; the gate electrodes within successive pixel rows belonging to each coset of modulo 16 [wherein  $N = 16$ ], 16 being a predetermined natural number between 4 and one half the number of pixels [with the number of pixels  $\geq 32$ ] in a column, and a minimum number of 16 corresponding to a periodic unit of gate electrode connections to the connection terminals within the successive pixel rows, the gate electrodes being combined with 16 gate electrode groups to reduce the number of the connection terminals (see Page 2, Line 15 - Page 5, Line 6; wherein the number of connection terminals has been reduced to 16, as opposed to utilizing a separate external connection terminal for each individual gate electrode).

Regarding claim 2, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses gate electrodes/gate control lines [Fig. 7, 4A] within successive pixel rows belonging to each coset of modulo 16 [wherein  $N=16$ ], 16 being combined with each other so as to reduce the number of the connection terminals (see Page 2, Line 15 - Page 5, Line 6; wherein the number of external connection terminals has been reduced to 16, rather than utilizing a separate external connection terminal for each individual gate electrode).

Regarding claim 3, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the gate electrodes being provided in a predetermined number 32 [wherein  $N = 32$ ], 32 being a predetermined natural number between 4 and one half the number of pixels [with the number of pixels = 64] in a column, of gate electrode groups such that the horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo 32, some of the gate electrode groups being commonly connected so that the connection electrodes are less in number than 32 (see Page 2, Line 15 - Page 5, Line 6; wherein there are provided 16 external connection terminals for 32 gate electrode groups of 2 pixels each, for a grand total of 64 pixels).

Regarding claim 4, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving (see Fig. 7; Page 4, Line 8 - Page 5, Line 6).

Regarding claim 5, this claim is rejected under the reasoning applied in the above rejection of claims 1, 2 and 4.

Regarding claim 6, this claim is rejected under the reasoning applied in the above rejection of claims 1, 3 and 4.

Regarding claims 7-9, the background of the current invention discloses gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit (see Fig. 7; Page 4, Line 8 - Page 5, Line 6; wherein 16 connection terminals is the minimum for this particular display device).

Regarding claim 10, his claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the gate electrodes within successive pixel rows belonging to each coset of modulo 16 [wherein  $N = 16$ ], 16 being a predetermined natural number between a minimum number corresponding to shared connections between some gate electrode groups to the connection terminals within the successive pixel rows and a maximum number corresponding to one half the number of pixels [with the number of pixels  $\geq 32$ ] in a column, being combined with 16 gate electrode groups to reduce the number of connection terminals (see Page 2, Line 15 - Page 5, Line 6; wherein the number of connection terminals has been reduced to 16, as opposed to utilizing a separate external connection terminal for each individual gate electrode).

### ***Response to Arguments***

8. Applicants' arguments filed April 15, 2002 have been fully considered but they are not persuasive. The applicants contend that the purported prior art of Figure 7 does not teach sharing connection electrodes by electrodes from different gate electrode groups. The examiner

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respectfully disagrees. Figure 7 illustrates using separate connection terminals [Fig. 7, 6] for each shift gate [Fig. 7, 3] of sixteen unique pixels [Fig. 7, 1]. However, Figure 7 further illustrates that the shift gate of every 16th pixel is commonly connected to the 16th connection terminal (via the gate electrodes [Fig. 7, 4A]). In this manner, the background of the current invention does disclose the sharing of connection electrodes by electrodes from different gate electrode groups.

The applicants also contend that the purported prior art does not teach gate electrode groups being commonly connected so that the number of connection terminals is less than the number the electrode groups. The examiner again respectfully disagrees. Although Figure 7 only numbers the pixels 1-16, there are in fact 17 total pixels shown (i.e. there are two #16 pixels). Figure 7 teaches connecting connection terminal #16 to both #16 pixels. Thereby, only sixteen connection terminals are used to control 17+ pixels. In this manner, the purported prior art does teach gate electrode groups being commonly connected so that the number of connection terminals is less than the number the electrode groups.

By such reasoning, the rejection of claims 1-10 is deemed proper and thereby maintained.

### ***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

  
J.P.

July 15, 2002

  
BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
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